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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Takeshi Nogami	:	Confirmation No.:	7243
Serial No.:	09/579,340	:	Art Unit:	2814
Filed:	5/25/2000	:	Examiner:	Vikki H. Trinh
For:	INTEGRATED CIRCUIT CHIP WITH HIGH-ASPECT RATIO VIAS	:		

Commissioner for Patents
Washington, D. C. 20231

APPEAL BRIEF

Sir:

The following Appeal Brief is submitted pursuant to the Notice of Appeal filed January 2, 2003 in the above identified Application.

(1) ***Real party in interest:***

The real party in interest is Advanced Micro Devices, Inc. of One AMD Place, P.O. Box 3453, Sunnyvale, CA 94088-3453.

(2) ***Related appeals and interferences:***

There are no known related appeal or interference cases.

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(3) ***Status of claims:***

Claims 1-20, the only claims pending, stand under final rejection from which rejection this Appeal is taken.

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(4) ***Status of amendments:***

No amendments have been filed subsequent to the final rejection of October 2, 2002.

(5) ***Summary of invention:***

The present invention is an integrated circuit chip including a semiconductor substrate [100] with a semiconductor device [112]. A dielectric layer [110,122] is formed having a channel opening [103] and a via [105]. The via [105] having a via entrant angle [70] formed with the channel opening [103] of greater than about 69 degrees whereby said channel opening [103] forms a collimator for the via [103]. A seed layer [146] lines the channel opening [103] and the via [105]. A conductive layer [107] is damascened into the seed layer [146] and the dielectric layer [110] whereby the conductive layer [107] in said channel opening [103] is operatively connected by the conductive layer [107] in the via [105] to the semiconductor device [112] without voids.

(6) ***Issues:***

Issue 1:

Whether a suggestion, teaching, or motivation to combine prior art references is an essential component of an obviousness holding.

Issue 2:

Where there is no motivation articulated for combining the references, it is not obvious to those skilled in the art to combine the references, and the applicant requests an Examiner Affidavit pursuant to 37 CFR §1.104(d)(2) (2002) disclosing the Examiner's personal knowledge being used to combine the references, whether the Examiner may respond by repeating the applicant's remarks are not persuasive, repeating the Examiner has established a prima facie case by paraphrasing portions of the claim, and concluding the applicant's argument is moot.

Issue 3:

Whether claims 1-20 are rejected under 35 USC §103(a) as being obvious over admitted prior art (FIGs. 1A-1C and Specification pages 1-7, hereinafter "APA") in view of Wang et al. (USPN 5, 629, 237, hereinafter "Wang").

(7) ***Grouping of claims:***

With respect to the ground of rejection under 35 USC §103(a) claims 1, 2, 10-12, and 20 stand or fall separately, claims 3-9 stand or fall together, and claims 13-19 stand or fall together.

(8) ***Arguments:***

Issue 1:

Whether a suggestion, teaching, or motivation to combine prior art references is an essential component of an obviousness holding.

In the Examiner's Final Rejection of 10/02/2002, Page 3, in the paragraph starting at line 13, the Examiner states the standard of obviousness she is applying to the present invention:

> "The courts have concluded that there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170 USPQ 209 (CCPA 1971). Also, references are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA 1969)." [underlining for clarity]

The above is believed to be an obsolete standard. On January 18, 2002, the Court of Appeals for the Federal Circuit (CAFC) vacated a judgment of the Board of Patent Appeal and Interferences in *In re* Sang-Su Lee, 277 F.3d 1338 (Fed. Cir. 2002) because the Board had erroneously held that "the conclusion of obviousness may be made from common knowledge and common sense of a person of ordinary skill in the art without any specific hint or suggestion in a particular reference." This conclusion is analogous to the standard the Examiner is applying in relying on *In re* McLaughlin, supra.

The Court held that a showing of a suggestion, teaching, or motivation to combine prior art references is an essential component of an obviousness holding. The Court emphasized that this need for specificity pervades precedential authority and reinforced the requirement that teachings of references can be combined only if there is some suggestion or incentive to do so (*In re* Fine, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988)).

That precedential authority includes: Brown & Williamson Tobacco Corp. v. Philip Morris Inc., 229 F.3d 1120, 1124-25, 56 USPQ2d 1456, 1459 (Fed. Cir. 2000) ("a showing of a suggestion, teaching, or motivation to combine the prior art references is an 'essential component of an obviousness holding'") (quoting C.R. Bard, Inc., v. M3 Systems, Inc., 157 F.3d 1340, 1352, 48 USPQ2d 1225, 1232 (Fed. Cir. 1998)); In re Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999) ("Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references."); In re Fine, supra ("'teachings of references can be combined only if there is some suggestion or incentive to do so.'") (underline in original) (quoting ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984)).

The current requirement for a prima facie case of obviousness under 35 USC §103 is that there must be:

> "...some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." (*In re* Fritch, 972 F.2d 1260, 23 USPQ 2d 1780, 1783 Fed. Cir. 1992). [underlines added]

Further, *In re* Dance, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998), states there must be some motivation, suggestion, or teaching of the desirability of making the specific combination that was made by the applicant.

The above are more recent than and directly contrary to *In re* McLaughlin, a 1971 CCPA case and to *In re* Bozek, a 1969 CCPA case.

Since the Examiner has impliedly concluded in the Final Rejection of 10/02/2002 page 3, lines 13-14, that there is no motivation expressly articulated in either reference, there must either be no motivation or the motivation must be based on the Examiner's personal knowledge so an Examiner Affidavit pursuant to 37 CFR §1.104(d)(2) (2002) disclosing the Examiner's personal knowledge was requested. No Examiner Affidavit has been provided.

Issue 2:

Where there is no motivation articulated in the references for combining the references that is obvious to those skilled in the art and the applicant requests an Examiner Affidavit pursuant to 37 CFR §1.104(d)(2) (2002) disclosing the Examiner's personal knowledge being used to combine the references, the Examiner may respond by stating conclusions as fact as in the Advisory Action of 01/02/2003, item 5:

> "[A]pplicant's argument is not persuasive. Applicant argues that the examiner uses obsolete law, in particular the cited cases law, Graham v. John Deere Co (1969), In re McLaughlin (1971), and In re Bozek (1969). On the contrary, the cited cases are still applicable and are used to supplement applicant's understanding of the obviousness rejection under 35 USC 103(a)."

Unobviousness under Deere was specifically traversed in Appellant's Amendment After Final of March 11, 2002:

> "The Examiner summarizes the criteria for determining obviousness under 35 USC 103(a) based on the considerations established in Graham v. John Deere Company, 383 US 1, 148 USPQ 459 (1966).
>
> It is respectfully submitted that all four Graham v. John Deere Company factors show the nonobviousness of Applicant's claims as explained in the Applicant's Response of December 12, 2001, which is incorporated herein by reference thereto. Essentially, with regard to:
>
> 1. Determining the scope and contents of the prior art: The scope and contents of APA disclose a rectangular channel intersecting with a cylinder with no particular relationship and Wang discloses a beveled via.
> 2. Ascertaining the differences between the prior art and the claims at issue: APA and Wang do not teach or suggest a collimeter structure between the channel opening and the via opening.
> 3. Resolving the level of ordinary skill in the pertinent art: Those of ordinary skill in the pertinent art would be those skilled in the semiconductor device manufacturing art who have been unable to solve the problem solved by the Applicant's claimed invention.
> 4. Considering the objective evidence present in the application indicating obviousness or nonobviousness: The application indicates that a solution to uniform formation of seed layers in vias has long eluded those skilled in the art and thus that the Applicant's claimed invention is unobvious.
>
> Therefore, it is respectfully submitted that Applicant's claimed invention is unobvious under Graham v. John Deere Company."

And the more recent test for combining references was explained for Issue 1 above which is contrary to In re McLaughlin and In re Bozek.

The Examiner continued in the Advisory Action:

> "The examiner has established the prima facie case of obviousness in the rejection. In particular, as stated in the final rejection, an artisan having ordinary skilled (sic) in the art at the time the invention was made would have been (sic) readily applied the entrant angle of APA with the overlapping range of the entrant angle of more than 69 degrees, as taught by Wang, so as to provide law resistance contacts. (see column 3, line 1.) Therefore, applicant's argument is moot."

It is respectfully submitted that the Examiner is not permitted to establish a prima facie case merely by stating:

> "The admitted prior art and Wang et al. '237 are in the same field of endeavors.
> Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to..."

The above is the only basis of obviousness set forth in both the Office Action of 09/12/01 and the Final Rejection 01/11/02.

Appellant traversed the above basis of rejection as legally insufficient as indicated above, traversed the obviousness of the combination as shown below and, since the combination did not appear to be obvious to those skilled in the art, repeatedly requested an Examiner Affidavit pursuant to 37 CFR §1.104(d)(2) (2002) disclosing the Examiner's personal knowledge. 37 CFR §1.104(d)(2) (2002) states:

> "When a rejection in an application is based on facts within the personal knowledge of an employee of the Office, the data shall be as specific as possible and the reference must be supported, when called for by the applicant, by the affidavit of such employee, and such affidavit shall be subject to contradiction or explanation by the affidavits of the applicant and other persons." [underlining for clarity]

No further explanation other than that in the Advisory Action has been provided. Also, no Examiner Affidavit has been provided.

The Examiner bears the burden of establishing a prima facie case of obviousness. As stated by the Federal Circuit in *In re* Oetiker, 977 F.2d 1443, 24 USPQ 2d 1443, 1447 (Fed. Cir. 1992):

> "The examiner cannot sit mum, leaving the applicant to shoot arrows in the dark hoping to somehow hit a secret objection harbored by the examiner. The prima facie case notion...seemingly was intended to leave no doubt among examiners that they must state clearly and specifically any objections (the prima facie case) to patentability and give the applicant fair opportunity to meet those objections with evidence and argument. To that

extent the concept serves to level the playing field and reduces the likelihood of administrative arbitrariness." [deletion for clarity]

It is respectfully submitted that the Examiner has failed to bear the burden of establishing a prima facie case.

Issue 3:

Claims 1-20 are rejected under 35 USC §103(a) as being obvious over admitted prior art (FIGs. 1A-1C and Specification pages 1-7, hereinafter "APA") in view of Wang et al. (USPN 5, 629, 237, hereinafter "Wang").

Summary of APA:

APA discloses the problematic structure in which an integrated circuit chip includes a semiconductor substrate [100] with a semiconductor device [112]. A dielectric layer [110,122] is formed having a channel [104] and a via [106], which are randomly sized. A seed layer [128] lines a channel and via opening. The seed layer thickness is much higher in wide-open areas, such as on top of a via dielectric layer [122] and in the upper portion of the via [106]. To guarantee a minimum seed layer thickness at the bottom of the via [106], the seed layer thickness in the wide-open areas tends to be much thicker. An overhang [129] is created by the fusibility of the conductive material of the seed layer [128 and an adhesion/barrier layer 126 at the rim of the via opening. An excessively thick seed layer in the upper portion of the via [106] interferes with the subsequent filling of the via [106] and causes a void [130]. [APA FIG. 1C, page 5, line 23, through page 6, line 13]

Summary of Wang:

Wang discloses a dielectic layer with a tapered contact via hole in which the via hole has a bevel where the entrance of the bevel into the via hole is less than 90°. [Wang Abstract, Wang col. 1, lines 31-33]

Appellant respectfully traversed the rejections since the Appellant's claimed combination, as exemplified in claim 1, includes the limitation not disclosed in APA or Wang of:

> "...a dielectric layer formed over said semiconductor substrate and said semiconductor device, said dielectric layer having a channel opening and a via provided therein; said via having a via entrant angle formed with said channel opening of greater than about 69 degrees..." [underlining for clarity]

Based on the above, the Appellant's claimed invention requires a channel and a via because the Appellant's via entrant angle is defined by a line connecting the rim of the channel and the rim of the via. This may be seen with reference to FIG. 2 and Specification page 7, lines 21-25, which states:

> "In the present invention, the second channel opening 103 is configured so that its width at the rims 134 form the via entrant angle 69 with the rim 132 of the via opening 105. This causes the rims 134 to act as a collimator for subsequent plasma or ion deposition processes where the deposition of the second adhesion/barrier layer 138 requires this "channel collimator effect"."

Appellant respectfully traversed the rejections since the Appellant's claimed combination, as exemplified in claim 1, also includes the limitation not disclosed in APA or Wang of:

> "...whereby said channel opening forms a collimator for said via..."

Based on the above, the Appellant's claimed invention requires the channel form a collimator for the via. A collimator is a device or structure for producing a particle beam, such as an ionized metal plasma, in which all the particle paths are substantially parallel.

The APA discloses an integrated circuit chip having a rectangular channel intersecting a cylindrical via (FIGs. 1A-C and specification pages 1-7). APA discloses on Specification page 3, lines 10-20, the problems with APA in that:

> "The common problems associated with most of the seed layer deposition techniques are poor sidewall step coverage and conformality, i.e., the seed layer thickness is much higher in wide-open areas, such as on top of the channel oxide layer, in the upper portion of the sidewalls of the channels and vias, and bottom of the channels than in the lower portion of the sidewalls of the channels and vias. To guarantee a minimum seed layer thickness anywhere in the channel or vias, including at the lower portion of the sidewalls, the seed layer thickness in wide-open areas tends to be much higher. As the width of the channels and vias have decreased in size due to the size reduction in the semiconductor devices, an excessively thick seed

> layer in the wide-open areas interferes with the subsequent filling of the channel and vias with conductive materials leading to the formation of voids. These voids lead to connection and electro-migration failures."

Based on the above, APA has problems with guaranteeing seed layer thickness in view of the decreasing width of the channels and vias. There is no suggestion of any particular relationship between the channels and the vias or the channel opening and the via opening.

Wang does not disclose a channel or seed layer but discloses a cylindrical via having a bevel or taper intersecting a planar surface; i.e., a cylindrical via having a conical opening such that the top of the via has a larger diameter than the bottom of the via. The angle of the bevel of the via relative to the top of the via is the Wang "angle of entrance". The Wang via is formed in a number of steps as follows as disclosed in Wang col. 3, lines 39-64, through:

> "Refer now to FIG. 2 through FIG. 6, ...a method of forming a tapered contact via hole with a high aspect ratio. ...
> ...FIG. 2, a first via hole opening 32 is then formed in the insulating layer 30
> ...FIG. 3, the first via hole opening is extended to form a second via hole opening 34
> ...FIG. 4, the second via hole opening is extended to form a third via hole opening.
> ... FIG. 5, the third via hole opening is extended to form the contact via hole 38.
> ...FIG. 6, ...the formation of the contact via hole 38 is completed. In this case there is no re-entrance profile formed at the entrance to the contact via hole and the angle of entrance 54 into the contact via hole is substantially less than 90°...."

From the above, it is apparent that Wang first creates a hemispherical first via opening 32 under a masking layer 40, extends the hemispherical opening downward with a cylindrical opening 34, forms a more conical opening 36, and then finishes with a cylindrical opening through the bottom of the conical opening. This leaves a beveled cylindrical via.

Based on the above under Graham v. John Deere Co., 383 Us 1, 148 USPQ 459 (Sup. Ct. 1966), the four factual inquiries would be resolved as follows:

The scope and contents of APA disclose a rectangular channel intersecting with a cylinder with no particular relationship and Wang discloses a beveled via.

The differences between the prior art and the claims at issue indicate that the Appellant's claimed limitation of a structure having a via entrant angle are not disclosed in

APA. In Wang, without a channel, it cannot have a via entrant angle as claimed by Appellant. Taking APA and adding the Wang channel will result in a beveled cylinder via intersecting a rectangular channel. Since the beveled cylinder takes up more space than a non-beveled cylinder, this would be non-obvious because it would defeat the objective in APA of reducing the spacing between the channels and vias.

The differences between the prior art and the claims at issue indicate that the Appellant's claimed limitation of a collimeter does not exist in APA. In Wang, there is no disclosure of a structure to cause the particles of an ionized metal plasma to enter the via in parallel because the non-parallel plasma is blocked out by a separate structure such as the walls of the channel in Appellant's invention.

Resolving the ordinary skill in the art would indicate one having ordinary skill in semiconductor device manufacture. APA admits the unobviousness of the Appellant's invention on Specification page 3, lines 21-25, which states:

> "A solution, which would form uniform seed layers in vias and result in an improvement in the subsequent filling of the vias by conductive materials, has long been sought, but has eluded those skilled in the art. As the semiconductor industry moves from aluminum to copper and other types of high conductivity materials, it is becoming more pressing that a solution be found."

Wang admits that it is concerned with forming a beveled hole by stating in Wang col. 1, lines 31-33:

> "The importance of beveled contact holes has been recognized for some time and many have worked on methods of achieving them."

It is respectfully submitted that Appellant's invention does not disclose a beveled contact hole and the angle of entrance of the via Appellant's invention would be described as 90° since there is no bevel.

In considering the objective evidence present in the application indicating obviousness or unobviousness, it is respectfully submitted that this should be resolved in favor of unobviousness because neither APA nor Wang discloses Appellant's claimed entrant angle or collimator structure.

It is submitted that the combination of APA and Wang would teach a channel having a beveled opening into a cylindrical opening would be taught away from since the conical

openings would prevent the vias from being placed close together and therefore prevent decreased size in semiconductor devices.

Based on the above and even applying the factual inquiry set forth in Graham v. John Deere Co., 383 US 1, 141 USPQ 459 (SUP. CT. 1966), all four factors would mitigate towards the unobviousness of Appellant's claims.

It is respectfully submitted that a prima facie case of obviousness under 35 USC §103 cannot be made for claims 1 because there is nothing to suggest the combination. As explained in *Laitram Corp. v. Cambridge Wire Cloth Co.*, 226 USPQ 298 at 293n (D. Md. Mag. 1985), aff'd in part, rev'd in part, and remanded, 785 F.2d 292, 228 USPQ 935 (Fed. Cir. 1986), cert. denied, 479 U.S. 820 (1986):

> "The question is whether the prior art, considering its scope and content and the level of ordinary skill, must itself suggest the combination of separate elements into the claimed invention in suit, not just whether it illustrates separate elements..." [underlining for clarity]

It is respectfully submitted that APA and Wang in combination do not teach or suggest the Appellants' claimed invention as required by 35 USC §103(a) under the proper standard of review, that they individually teach away from Appellant's claimed invention under 35 USC §103(a), and that they teach away from combination with each other such that a prima case of obviousness cannot be made under 35 USC §103(a).

With regard to claim 2, it is respectfully submitted that APA does not teach or suggest a having an adhesion/barrier layer via entrant angle formed with an adhesion/barrier layer channel opening of greater than about 70 degrees whereby said adhesion/barrier channel opening forms a collimator for said adhesion/barrier layer via and Wang does not teach or suggest an adhesion/barrier layer or a an adhesion/barrier layer channel opening. Therefore, there is no teaching or suggestion for a combination which includes the claim limitation of:

> "an adhesion/barrier layer disposed between said dielectric layer and said seed layer in said channel opening and said via, said via with said adhesion/barrier layer having an adhesion/barrier layer via entrant angle formed with an adhesion/barrier layer channel opening of greater than about 70 degrees whereby said adhesion/barrier channel opening forms a collimator for said adhesion/barrier layer via."

With regard to claim 3-9, the dependent claims stand or fall together with claim 1.

With regard to claim 10, this dependent claim is believed to be allowable because APA discloses a non-uniform thickness in the channel opening and the via while Wang does not even teach or suggest a channel opening. Therefore, there is no teaching or suggestion for a combination which includes the claim limitation:

> "said seed layer is of a relatively uniform thickness in said channel opening and said via."

With regard to claim 11, this independent claim is believed to be allowable for the same reasons as given for claim 1.

With regard to claim 12, this dependent claim is believed to be allowable for the same reasons as given for claim 2.

With regard to claims 13-19, they stand or fall together with claim 11.

With regard to claim 20, this dependent claim is believed to be allowable for the same reasons as given for claim 10.

Based on all of the above, claims 1-20 are patentable under 35 USC §103(a) as being unobvious based on APA in view of Wang.

(9) Conclusion and Relief Requested

The claims 1-20 are patentable over the prior art.

Reversal of the Examiner's decision is respectfully requested.

Respectfully submitted,

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Date: March 3, 2003

Appendix A - Claims on Appeal (On following pages)

Appendix A - Claims on Appeal

1. An integrated circuit chip comprising:

a semiconductor substrate;

a semiconductor device over said semiconductor substrate;

a dielectric layer formed over said semiconductor substrate and said semiconductor device, said dielectric layer having a channel opening and a via provided therein, said via having a via entrant angle formed from a rim of said channel opening to a rim of the via and a horizontal bottom of the channel opening of greater than about 69 degrees whereby said channel opening forms a collimator for said via and a depth and a cross-sectional area of the channel opening are determined by the via entrant angle;

a seed layer lining said channel opening and said via; and

a conductive layer damascened into said seed layer and said dielectric layer whereby said conductive layer in said channel opening is operatively connected by said conductive layer in said via to said semiconductor device without voids.

2. The integrated circuit chip as claimed in claim 1 including:

an adhesion/barrier layer disposed between said dielectric layer and said seed layer in said channel opening and said via, said via with said adhesion/barrier layer having an adhesion/barrier layer via entrant angle formed with an adhesion/barrier layer channel opening of greater than about 70 degrees whereby said adhesion/barrier channel opening forms a collimator for said adhesion/barrier layer via.

3. The integrated circuit chip as claimed in claim 2 including:

said adhesion/barrier layer deposited by a process selected from a group comprising physical vapor deposition, chemical vapor deposition, and a combination thereof.

4. The integrated circuit chip as claimed in claim 3 wherein:

said adhesion/barrier layer of a material selected from a group comprising titanium, tantalum, tungsten, titanium nitride, tantalum nitride, tungsten nitride, and a combination thereof.

5. The integrated circuit chip as claimed in claim 1 wherein:
said seed layer is formed by ionized metal plasma deposition.

6. The integrated circuit chip as claimed in claim 5 wherein:
said seed layer is formed of a material selected from a group comprising aluminum, copper, gold, silver, an alloy thereof, and a combination thereof.

7. The integrated circuit chip as claimed in claim 6 wherein:
said conductive layer is deposited by a process of electroplating.

8. The integrated circuit chip as claimed in claim 1 wherein:
said conductive layer is formed of a material selected from a group comprising aluminum, doped polysilicon, copper, gold, silver, an alloy thereof, and a combination thereof.

9. The integrated circuit chip as claimed in claim 1 wherein:
said via has a high-aspect ratio.

10. The integrated circuit chip as claimed in claim 1 wherein:
said seed layer is of a relatively uniform thickness in said channel opening and said via.

11. An integrated circuit chip comprising:
a semiconductor substrate;
a semiconductor device on said semiconductor substrate;
a first channel dielectric layer formed over said semiconductor substrate and said semiconductor device, said first channel dielectric layer having a first channel opening provided therein;
a first seed layer lining said first channel opening in said first channel dielectric layer;
a first conductive layer damascened into said first seed layer and said first channel dielectric layer whereby said conductive layer in said first channel opening is operatively connected to said semiconductor device;
second channel and via dielectric layers formed over said first channel dielectric layer, said second channel and via dielectric layers having a second channel opening and a via provided therein, said via having a via entrant angle formed from a rim of said second channel opening to a rim of the via and a horizontal bottom of the channel opening of greater than about 69 degrees whereby said

second channel opening forms a collimator for said via and a depth and a cross-sectional area of the second channel opening are determined by the via entrant angle;

a second seed layer lining said second channel opening and said via; and

a second conductive layer damascened into said second seed layer and said second channel dielectric and via layers whereby said second conductive layer in said second channel opening is connected by said second conductive layer in said via to said first conductive layer in said first channel without voids.

12. The integrated circuit chip as claimed in claim 11 including:

a second adhesion/barrier layer disposed between said second channel dielectric layer and said second seed layer in said second channel opening and said via, said via with said adhesion/barrier layer having an adhesion/barrier layer via entrant angle formed with an adhesion/barrier layer channel opening of greater than about 70 degrees whereby said adhesion/barrier channel opening forms a collimator for said adhesion/barrier layer via.

13. The integrated circuit chip as claimed in claim 12 including:

said second adhesion/barrier layer deposited by a process selected from a group comprising physical vapor deposition, chemical vapor deposition, and a combination thereof.

14. The integrated circuit chip as claimed in claim 13 wherein:

said second adhesion/barrier layer of a material selected from a group comprising titanium, tantalum, tungsten, titanium nitride, tantalum nitride, tungsten nitride, and a combination thereof.

15. The integrated circuit chip as claimed in claim 11 wherein:

said second seed layer is formed by ionized metal plasma deposition.

16. The integrated circuit chip as claimed in claim 15 wherein:

said second seed layer is formed of a material selected from a group comprising aluminum, copper, gold, silver, an alloy thereof, and a combination thereof.

17. The integrated circuit chip as claimed in claim 16 wherein:

said second conductive layer is deposited by a process of electroplating on said second seed layer.

18. The integrated circuit chip as claimed in claim 11 wherein:

said second conductive layer is formed of a material selected from a group comprising aluminum, doped polysilicon, copper, gold, silver, an alloy thereof, and a combination thereof.

19. The integrated circuit chip as claimed in claim 11 wherein:

said via has a high-aspect ratio of diameter to depth in excess of 1:2.

20. The integrated circuit chip as claimed in claim 11 wherein:

said second seed layer is of a relatively uniform thickness in said second channel opening and in said via.